

EXHIBIT 3

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.,)	
)	
Plaintiff,)	
)	
vs.)	Civil Action No. 2:22-CV-203-JRG
)	
MICRON TECHNOLOGY, INC., MICRON)	JURY TRIAL DEMANDED
SEMICONDUCTOR PRODUCTS, INC.,)	
AND MICRON TECHNOLOGY TEXAS)	Filed Under Seal
LLC,)	
)	
Defendants.)	

**PLAINTIFF NETLIST, INC.’S FIRST NOTICE OF DEPOSITION OF DEFENDANTS
MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC.,
AND MICRON TECHNOLOGY TEXAS LLC**

Please Take Notice that, pursuant to Rule 30(b)(6) of the Federal Rules of Civil Procedure, and the Local Rules of this Court, Plaintiff Netlist, Inc. (“Netlist”) directs the following interrogatories to defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively “Micron” or “Defendants”). The deposition(s) shall take place at a mutually agreeable place and date, beginning at 9:00 am and continuing from day-to-day thereafter (excluding Saturdays, Sundays, and holidays) until completed. The deposition(s) will be conducted pursuant to the Federal Rules of Civil Procedure and will be conducted in the English language before a notary public or other officer authorized to administer oaths. The deposition(s) may be recorded by stenographic means, audiotaped, videotaped, and/or transcribed using real time interactive transcription (e.g., LiveNote).

Pursuant to Federal Rule of Civil Procedure 30(b)(6), Micron shall designate one or more of its officers, directors, managing agents, or other persons who are most knowledgeable, and competent to testify on its behalf, as to all matters known or reasonably available to Micron with

respect to the topics set forth in Attachment A. Pursuant to Federal Rule of Civil Procedure 30(b)(6), the person(s) designated should be prepared to testify as to such matters known or reasonably available to Micron. At least five (5) business days before the date set for the deposition(s), Micron shall identify, by name and position, each person so designated and shall set forth the matters on which that person will testify.

Netlist reserves the right to serve Micron with additional notices pursuant to Rule 30(b)(6) on additional topics as this litigation progresses and as further evidence is produced.

Dated: May 15, 2023

Respectfully submitted,

/s/ Jason G. Sheasby

Samuel F. Baxter
Texas State Bar No. 01938000
sbaxter@mckoolsmith.com
Jennifer L. Truelove
Texas State Bar No. 24012906
jtruelove@mckoolsmith.com
MCKOOL SMITH, P.C.
104 East Houston Street Suite 300
Marshall, TX 75670
Telephone: (903) 923-9000
Facsimile: (903) 923-9099

Jason G. Sheasby (*pro hac vice*)
jsheasby@irell.com
Annita Zhong, PhD (*pro hac vice*)
hzhong@irell.com
Thomas C. Werner (*pro hac vice*)
twerner@irell.com
Yanan Zhao (*pro hac vice*)
yzhao@irell.com
Michael W. Tezyan (*pro hac vice*)
mtezyan@irell.com

IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
Tel. (310) 277-1010
Fax (310) 203-7199

Attorneys for Plaintiff Netlist, Inc.

ATTACHMENT A

DEFINITIONS

Unless the context indicates otherwise, for purposes of these discovery requests, the following words and phrases have the meanings given:

1. “You,” “Your,” “Micron,” or “Defendant(s)” means Micron Technology, Inc., Micron Semiconductor Products, Inc., Micron Technology Texas LLC and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Micron, and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

2. “Netlist” shall mean Netlist, Inc. and all of its affiliates, officers, employees, agents, representatives, contractors, consultants, attorneys, successors, and assigns.

3. “Patent” shall mean any United States, international, or foreign classes or types of patents, utility models, design patents, applications (including provisional applications), certificates of invention, reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof. The defined term Patent includes all stated categories of intellectual property regardless of whether those rights are presently expired or were ever adjudged invalid.

4. “Netlist Patents-in-Suit” means and refers to one or more of U.S. Patent Nos. 10,860,506 (“506 Patent”), 10,949,339 (“339 Patent”), 11,016,918 (“918 Patent”),

11,232,054 (“’054 Patent”), 8,787,060 (“’060 Patent”), and 9,318,160 (“’160 Patent”).

5. “Third Party” means any individual, entity, organization, partnership, or corporation that is not a party to this action.

6. “Micron Accused DDR4 LRDIMMs” shall include any and all Micron Double Data Rate 4 (“DDR4”) load reduced dual in-line memory modules (“LRDIMMs”), including ones that its customers further customize.

7. “Micron Accused DDR5 DIMMs” shall include any and all Micron Double Data Rate 5 (“DDR5”) dual in-line memory modules, including ones that its customers further customize.

8. “Micron Accused HBM Products” shall include any and all Micron HBM2, HBM2E, HBM3, or HBMnext high bandwidth memory products, including ones that its customers further customize.

9. “Micron Accused Products” shall mean any and all Micron Accused DDR4 LRDIMMs, Micron Accused DDR5 DIMMs, and Micron Accused HBM Products.

10. “Micron Distributor” shall include any person who Micron authorized to sell any Micron Accused Products.

11. “Micron Partner” shall include any customers of Micron’s Accused Products and any other third parties involved in the design, development, manufacture, testing, assembly, importation, distribution, sourcing, qualification, sale, or offer to sell Micron Accused Products.

12. “Micron Supplier” means a natural person or a business entity that supplies any component involved in the Micron Accused Products or assembled Micron’s Accused Products in whole or in part. For the purposes of this definition, a co-development relationship

or a fabrication relationship shall constitute one type of supplier relationship.

13. “Montage” means Montage, Inc. (d/b/a Montage Technologies, Inc.), Montage Technology, Inc., and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Montage, Inc. and Montage Technology, Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

14. “MPS” means Monolithic Power Systems, Inc. and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Monolithic Power Systems, Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

15. “Rambus” means Rambus Inc. and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Rambus Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons

consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

16. “Renesas” means Renesas Electronics America Inc. and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Renesas Electronics America Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

17. “TI” means Texas Instruments Incorporated and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Texas Instruments Incorporated, and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

18. “Richtek” means Richtek USA, Inc. and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Richtek USA, Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not

limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

19. “Anpec” means Anpec Technology Inc., and any present or former parent, subsidiary, division, subdivision, affiliated company, licensee, predecessor, or successor of Anpec Technology Inc., and any of its or their present or former officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning any factual matter or matters of opinion relating to any issues involved in the action.

20. “Standard(s)” means any technical standard created, authorized, controlled, and/or developed privately or unilaterally by a corporation, consortium, regulatory body, government, or standards setting organization.

21. “JEDEC” means the JEDEC Solid State Technology Association.

22. “Person” refers to any natural individual; any form of business entity including, but not limited to, any corporation, company, firm, general partnership, limited partnership, limited liability company, joint venture, proprietorship, business association, association, foundation, and legal entity; any directors, officers, owners, members, employees, agents, representatives, and attorneys of any of the foregoing; anyone else purporting to act on behalf of any such natural person or business entity; or any government entity, agency, officer, department, or affiliate.

23. “Source Code” means programming language statements that can be compiled, transformed, interpreted, executed, or otherwise processed by software (or further compiled,

transformed, interpreted, executed, or otherwise processed by software) into object code. This includes, without limitation, instructions, statements, procedures, subroutines, and programs written in a high-level programming language, design description language, or assembly language, and Specifications (defined above) for the operation of hardware, including, without limitation, code written in languages such as VHDL, register-transfer language (RTL), and verilog, and firmware and technical documentation.

24. “Prior Art” is used in the same manner in which the term is used in pre-AIA 35 U.S.C. §§ 102 and 103, and includes any patent, printed publication, system, prior knowledge, prior use, prior sale, offer of sale, or other act or event relevant to patentability under 35 U.S.C. §§ 102 or 103, or that You otherwise assert renders any asserted claim invalid.

25. “Data Buffer” means data buffers for use in Micron Accused DDR4 LRDIMMs.

26. “RCD” means register clock drivers (“RCD”) for use in Micron Accused DDR4 LRDIMMs.

27. “DDR4 LRDIMM Write Buffer Timing Control Features” includes the following: (1) the tristate buffers in each Data Buffer for a write operation (“Write Tristate Buffers”); (2) the time period during which Write Tristate Buffers are enabled to drive write data to one or more associated data lines connecting to one or more associated DRAMs and the time period during which the Write Tristate Buffers are disabled; (3) latency if any used to determine the time period(s) in (2); (4) signals generated by the RCD in association with driving write data from a DDR4 LRDIMM data buffer to a DRAM and enablement of Write Tristate Buffers, and associated circuitry; (5) signals received by and generated by the RCD

in association with a write operation, and associated circuitry; and (6) the number of bits passing through Write Tristate Buffers during each enablement period to a respective DRAM.

28. “DDR4 LRDIMM Read Buffer Timing Control Features” includes the following: (1) signals generated by the RCD in association with sampling and transmitting read data by a data buffer and associated circuitry; (2) amount of read strobe delay by the Data Buffer in response to one or more signals in (1); (3) mechanisms by which the Data Buffer determines the amount of delay to be applied to a read strobe, and signals and circuitry associated therewith; (4) clock signals received or outputted by the Data Buffer and the RCD and associated circuitry; (5) the width of the read data for each Data Buffer; (6) the tristate buffers in each Data Buffer for a read operation (“Read Tristate Buffers”) and the time period during which each Read Tristate Buffer is enabled to drive read data to a memory controller of a host system and the period during which the Read Tristate Buffer is disabled; and (7) determination of any latency associated with (6).

29. “DDR5 Power Management Features” means features related to DDR5 DIMMs’ on-board power management and voltage regulation functionality, including but not limited to (1) input voltage monitoring and regulation, including in response to over-voltage and under-voltage detection, (2) output voltage regulation and monitoring, the associated target output voltage for each voltage regulator (whether linear or switch mode) and the selective switching on or off of an output power supply; and (3) mechanisms and algorithms for input voltage regulation, including signals generated, power supply switch and register value update in response to detection of over-voltage or under-voltage for input voltage.

30. “HBM Load Reduction Features” means features related to the reduction of capacitive load in high-bandwidth memory products, including but not limited to (1) the arrangement of the TSVs (i.e., any structures allowing for electrical communication between

the buffer die and some but not all core dies) and (2) enablement/disablement of TSV drivers in the buffer die.

31. “Patented Features” means one or more of DDR4 LRDIMM Write Buffer Timing Control Features, DDR4 LRDIMM Read Buffer Timing Control Features, DDR5 Power Management Features, and HBM Load Reduction Features.

32. “Including” and “include” mean including without limitation, whether or not the phrase “without limitation” is explicitly stated.

33. The words “and” and “or” are terms of inclusion and not of exclusion and are to be construed conjunctively or disjunctively as necessary to bring within the scope of these requests for production any information which might otherwise be construed to be outside their scope.

34. The term “any” shall mean “any and all” and the term “all” shall mean “any and all.”

35. “Date” means the exact day, month and year if so ascertainable, or if not, the best approximation (including relationship to seasons and other events).

36. “Document” means any form of communication or representation, in any language fixed in any tangible medium, including every form of recording letters, words, pictures, sounds, or symbols, or combinations thereof by means such as handwriting, printing, photostatting, photographing, magnetic taping or writing, optically burning or encoding, or any other form of storing, compiling, or mechanically or electrically recording data onto any media including paper, film, plastic, magnetic tape, computer disks, compact discs (CDs), digital video discs (DVDs) and the like. For example, the term “Document” includes without limitation, correspondence, memoranda, notes, diaries, minutes, statistics, letters, telegrams,

contracts, reports, studies, checks, statements, tags, labels, invoices, brochures, periodicals, receipts, returns, summaries, pamphlets, books, notebooks, lab notebooks, invention disclosures, prospectuses, interoffice, and intra-office communications, offers, notations of any sort of conversations, working papers, applications, permits, surveys, indices, telephone calls, meetings, printouts, teletypes, telefax, telefax records, invoices, work sheets, graphic or oral representations of any kind (including without limitation, pictures, photographs, charts, microfiche, microfilm, videotape, audiotape, recordings, motion pictures, plans, drawings, surveys), and electronic or mechanical records or representations of any kind (including, without limitation, electronic mail or e-mail, Instant Messages, tapes, cassettes, discs, and recordings).

37. Every draft, version, revision, or non-identical copy of a “Document,” including copies that differ from the original because of hand notation(s), shall be considered a separate “Document,” as that term is used herein, but exhibits, appendices and attachments to a “Document” shall be considered part of the “Document” itself.

38. “Communications” means all written, oral, telephonic, or other inquiries, dialogues, discussions, conversations, interviews, correspondence, consultations, negotiations, agreements, understandings, meetings, letters, notes, advertisements, e-mails and all other Documents evidencing any transmittal of information or verbal or nonverbal interaction between persons and entities.

39. “Thing” means any tangible item, including without limitation, models, prototypes and samples of any device or apparatus or product.

40. The terms “relate to,” “reflecting,” “relating to,” “concerning,” or any variations thereof, shall mean relating to, referring to, concerning, mentioning, reflecting,

regarding, pertaining to, evidencing, involving, describing, discussing, commenting on, embodying, responding to, supporting, contradicting, constituting (in whole or in part), or between (as in the context of Communications), as the context makes appropriate.

41. The term “Identify” or “Identity” shall mean:

- (1) In connection with natural persons, their full names, titles and job description, and their present or last known business address and residence (designating which);
- (2) In connection with firms, partnerships, corporations, proprietorships, associations or other entities, their name, and their present or last known addresses of the principal place of business (designating which);
- (3) In connection with Documents, a description of the Document, setting forth its Date, title, format, nature, substance, author or over whose name it issued, addressee, and present custodian thereof, with such reasonable particularity as would be sufficient to permit the Document to be sought by subpoena duces tecum or under the provisions of Rule 34 of the Federal Rules of Civil Procedure;
- (4) In connection with oral statements and Communications: (i) the Date and location where they were made; (ii) the identity of each of the participants and witnesses thereto, and all others present; (iii) the medium of communication; and (iv) their substance.

42. “Key Technical Information” shall mean each and all of (1) read and write operations in Micron Accused Products; (2) structure and function of data buffers and RCDs in Micron Accused DDR4 LRDIMM Products; (3) control and enablement period of the write and read paths and corresponding tristate buffers in data buffers in Micron Accused DDR4 LRDIMM Products; (4) data sampling and transmissions by data buffers in Micron Accused DDR4 LRDIMM Products, signals involved therein and how the signals are generated, (5) information sent during and after training mode; (6) chip selection generation and signaling; (7) rank multiplication; (8) configuration, interconnections, and electrical communications of the die interconnects in Micron Accused HBM Products; (9) communication of data, control,

and address signals to the control die (e.g., buffer die or logic die) and the DRAM dies in Micron Accused HBM Products; (10) control of the driver sizes in Micron Accused HBM Products; (11) chip selection mechanisms in Micron Accused HBM Products; (12) interconnections between TSVs in DRAMs and I/O and power terminals in Micron Accused HBM Products; and (13) voltage regulation and power management in Micron Accused DDR5 Products, including identification of structures, components and operations thereof, type and amplitude of supply voltages to each component in Micron Accused DDR5 Products, and operation and signaling in Micron Accused DDR5 Products in over-voltage or under-voltage situations.

TOPICS

TOPIC NO. 1:

The identity of the three (3) most knowledgeable Persons for each category of Key Technical Information, including their dates of employment, current and previous titles, and qualification.

TOPIC NO. 2:

Micron's organizational structure with respect to the Micron Accused Products, including but not limited to the description of any research centers, groups, subdivisions, departments, or persons responsible for the design, development, engineering, testing, manufacture, assembly, distribution, sourcing, qualification, and distribution of Micron Accused Products and components thereof (such as data buffers, registering clock drivers, PMICs, and control dies).

TOPIC NO. 3:

The Identity, location, organizational structure, and responsibilities of each Micron person, group, team, business, or functional unit involved with the sales or marketing of

Micron Accused Products.

TOPIC NO. 4:

Micron's corporate structure and organization, including any relationship between or among Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC; Micron Partners, Distributors, and Suppliers (including without limitation to those disclosed in Micron's Initial Disclosures); any past or present successors, subsidiaries, divisions, parents, or affiliates of the same; and any joint ventures or other legal entities that Micron wholly or partially owns or owned, either directly or indirectly involved in the design, development, manufacture, testing, assembly, importation, distribution, sale, or offer to sell of Micron Accused Products.

TOPIC NO. 5:

The identification of all Micron Accused Products, including the meaning of Micron's product codes or part numbers.

TOPIC NO. 6:

Operations and structures of Micron's Accused HBM Products, including explanation of documents relating to the operation and structures of Micron's Accused HBM Products produced in this Action.

TOPIC NO. 7:

The TSV structure in Micron's Accused HBM Products, all alternatives that Micron considered, and the advantages and disadvantages for each alternative considered versus the adopted structure.

TOPIC NO. 8:

The read, write and repair operations in Micron's Accused HBM products, including signals received from the host, signals generated by the buffer die, signals exchanged between

the buffer die and core dies, data/control/address signal paths, and enablement and disablement of data paths in the read, write and repair operations.

TOPIC NO. 9:

Configuration, interconnections, and electrical communications of the die interconnects in Micron Accused HBM Products.

TOPIC NO. 10:

Communication of data, control, and address signals between the control die (e.g., buffer die or logic die) and the DRAM dies in Micron Accused HBM Products.

TOPIC NO. 11:

Control of the driver sizes in Micron Accused HBM Products.

TOPIC NO. 12:

Interconnections between TSVs in DRAMs and I/O and power terminals in Micron Accused HBM Products.

TOPIC NO. 13:

The capacitance and resistance of every electrical path carrying address, data, or control signals between control and buffer dies in each of Micron's Accused HBM Products, and each arrangement considered during the design process.

TOPIC NO. 14:

Operations and structures of Micron's Accused DDR5 Products, including explanation of documents relating to the operation and structures of Micron's Accused DDR5 Products produced in this Action.

TOPIC NO. 15:

Voltage regulation, operation states, and power management in Micron Accused DDR5 Products.

TOPIC NO. 16:

The operations and operating states of Micron's Accused DDR5 DIMMs when the input voltage to a PMIC is at or above an over-voltage threshold or at or below an under-voltage threshold, including the identification of (i) signals generated by PMICs; (ii) signals transferred between PMICs and host or between PMICs and other components on the memory module; (iii) any change in the operating state of other components on the memory module; (iv) any non-volatile memories that are updated; (v) any volatile memories that are updated; (vi) any other changes. If the resulting operations or operating states differ depending on the specific Micron Accused DDR5 DIMM or PMIC used, the separate description of each resulting operation and operating state.

TOPIC NO. 17:

For each PMIC used in Micron Accused DDR5 DIMMs, the identification of the voltage source (including the identification of the circuit that produces the voltage, the input to that circuit, and the output to the circuit) for (i) each non-PMIC component on the DDR5 DIMMs; and (ii) each PMIC functional block; and (iii) to the extent that voltage sources may change depending on the different operating conditions, the identification of any such changes in voltage source(s) (including the identification of the circuit that produces the voltage, the input to that circuit, and the output to the circuit), and the conditions that trigger those changes.

TOPIC NO. 18:

Operations and structures of Micron's Accused DDR4 LRDIMM Products, including explanation of documents relating to the operation and structures of Micron's Accused DDR4 LRDIMM Products produced in this Action.

TOPIC NO. 19:

Presence and/or absence of tristate buffers on data paths in Micron Accused DDR4

LRDIMM Products.

TOPIC NO. 20:

The start time and duration of time periods during which data paths and associated tristate buffers are enabled in Micron Accused DDR4 LRDIMM Products;

TOPIC NO. 21:

Information sent during and after training mode in Micron Accused DDR4 LRDIMM Products.

TOPIC NO. 22:

The amount of data strobe delay in data buffers in Micron Accused DDR4 LRDIMM Products for data sampling and how the amount of delay is determined.

TOPIC NO. 23:

For each DDR4 LRDIMM accused product, any buffer control words that affect the timing of the data for a write operation as it passes through a data buffer, including how the buffer control words affect when the data path for the write path through the data buffer is enabled or disabled, how the buffer control words affect the operation of the write FIFO on the data path, how the buffer control words affect the enablement or disablement of tristate buffers on the data path and the timing of the enablement/disablement, how the buffer control words affect the operation of the transmitters and receivers on the data path, and why the data path for the write data in the data buffer is turned off between write operations.

TOPIC NO. 24:

All facts and circumstances related to Micron's use in its DDR4 LRDIMM products of data buffers supporting the training modes described in JEDEC Standard 82-32A, DDR4 Data Buffer Definition (DDR4DB02), and any revisions thereof, including but not limited to: how DDR4 LRDIMM performance would be affected if the buffer control words in registers

F[3:0]BC4x or F[3:0]BC5x of a data buffer were not correctly set; how frequently MRD training is performed during a DDR4 LRDIMM's operation; reasons that Micron performs testing to ensure that Micron Suppliers' data buffers can correctly implement MRD training; whether, and reasons why, Micron uses any data buffers that do not comply with JEDEC Standard 82-32A, DDR4 Data Buffer Definition (DDR4DB02) and/or any revisions.

TOPIC NO. 25:

The read operations in Micron's Accused DDR4 LRDIMMs, including but not limited to (i) the signals received and sent by each component on the memory module; (ii) the electrical lines on which the signals are transmitted; (iii) the amount of delay that is applied to MDQS in a read operation; (iv) the buffer control words containing the information on the amount of delay described in (iii); (v) how the data buffer receives the value(s) of the control words of (iv); (vi) the mechanism by which data paths via which read data is transmitted through the data buffer ("read data paths") are enabled and disabled; (vii) the period during which the read data paths are enabled; (viii) the period during which the read paths are disabled; (ix) the signals and parameters used to control the enablement and disablement of the read data paths through the data buffer.

TOPIC NO. 26:

The write operations in Micron's Accused DDR4 LRDIMMs, including but not limited to (i) the signals received and sent by each component on the DIMM; (ii) the electrical lines on which the signals are transmitted; (iii) the mechanism by which write data paths via which write data is transmitted through the data buffer ("write data paths") are enabled and disabled; (iv) the period during which the write data paths are enabled; (v) the period during which the write data paths are enabled or disabled; and (vi) the signals and parameters used to control the enablement and disablement of the read data paths through the data buffer.

TOPIC NO. 27:

The structure and function of Micron's NVDIMM products, including in complete detail all power management features, including but not limited to (1) input voltage monitoring and regulation, including in response to over-voltage and under-voltage detection, (2) output voltage regulation and monitoring, the associated target output voltage for each voltage regulator (whether linear or switch mode) and the selective switching on or off of an output power supply; and (3) mechanisms and algorithms for input voltage regulation, including signals generated, power supply switch and register value update in response to detection of over-voltage or under-voltage for input voltage.

TOPIC NO. 28:

Micron's implementation and development of any method, structure, or functions described in the prior art references relied on in Your Invalidity Contentions, including Micron's implementation and development of the alleged Micron Hybrid Memory Cube System.

TOPIC NO. 29:

All facts relating to the competitive advantages and disadvantages of Micron's products compared with those of Micron's competitors, including any value Micron asserts is attributable to Micron Accused Products separate from the Patented Features.

TOPIC NO. 30:

The identity and location of Documents and Source Code as related to Key Technical Information and the identity of Persons having access to these Documents and Source Code.

TOPIC NO. 31:

The identity of Documents and Source Code that Micron receives from and/or shares with its Suppliers, Partners, and Distributors as related to the Micron Accused Products.

TOPIC NO. 32:

The identity of Documents and Source Code that Micron has a right to or has requested from its Suppliers, Partners, and Distributors as related to the Micron Accused Products.

TOPIC NO. 33:

The qualification and sourcing process for Micron's Accused Products, including Documents created during such process.

TOPIC NO. 34:

The relationship between Micron and any Micron Suppliers, Partners, Distributors, and other Third Parties involved in the design, development, manufacture, testing, assembly, importation, distribution, sale, or offer to sell of Micron Accused Products, including any related agreements, Micron's rights under the agreements, respective responsibilities, and contacts at Micron Suppliers, Partners, Distributors, and other Third Parties.

TOPIC NO. 35:

Explain the numbers and percentages of Micron Accused Products containing components supplied by third parties, including information for: (1) the respective numbers and percentages of Micron Accused DDR4 LRDIMMs containing data buffers supplied by Montage, Renesas, Richtek, Anpek, and/or other Micron Supplier(s); (2) the respective numbers and percentages of Micron Accused DDR4 LRDIMMs and Micron Accused DDR5 DIMMs containing RCDs supplied by Montage, Rambus, Renesas, Richtek, Anpec, and/or other Micron Supplier(s); (3) the respective numbers and percentages of Micron DDR5 RDIMMs containing power management integrated circuits ("PMICs") supplied by TI, MPS, Renesas, Richtek, Anpec, and/or other Micron Supplier(s); (4) the respective numbers and percentages of Micron DDR5 UDIMMs containing power management integrated circuits ("PMICs") supplied by TI, MPS, Renesas, Richtek, Anpec, and/or other Micron Supplier(s);

(5) the respective numbers and percentages of Micron DDR5 SODIMMs containing power management integrated circuits (“PMICs”) supplied by TI, MPS, Renesas, Richtek, Anpek, and/or other Micron Supplier(s); and (6) the respective numbers and percentages of Micron DDR5 DIMMs containing serial presence detect (“SPD”) supplied by Montage, Renesas, Richtek, Anpec, and/or other Micron Supplier(s).

TOPIC NO. 36:

The availability of any acceptable non-infringing alternatives to the inventions claimed in the Netlist Patents-in-Suit, including but not limited to identifying any alleged acceptable non-infringing alternative(s), identifying what Micron believes is the closest non-infringing alternative(s), and factual bases for the alleged acceptability and availability.

TOPIC NO. 37:

The customers of Micron’s Accused Products, including their identities, locations, main person(s) of contact for sales and qualification, long-term purchase agreements with Micron, purchase orders, price discounts, and sales records.

TOPIC NO. 38:

Micron’s customer base, market share, and distribution channels for Micron Accused Products.

TOPIC NO. 39:

Micron’s actual, proposed, contemplated, planned or prospective pricing policies, strategies, plans, practices, or decisions for Micron Accused Products.

TOPIC NO. 40:

Any benefits, financial or otherwise, that Micron receives, directly or indirectly, relating to Micron Accused Products.

TOPIC NO. 41:

The total units of Micron Accused Products sold or otherwise provided to customers from six years before the filing of this lawsuit to the present.

TOPIC NO. 42:

The gross revenues, net revenues, costs, gross profits, and net profits for each Micron Accused Product sold or otherwise provided to customers from six years before the filing of this lawsuit to the present.

TOPIC NO. 43:

Contracts or agreements entered by each Micron defendant with its customers in connection with the Accused Products, including information of: (1) the identity of each party involved; (2) location(s) where any contract, pricing, and projected demand were negotiated; (3) location(s) where any contract, pricing, and projected demand were executed; (4) location(s) where requests for proposals or bids are submitted; (5) location(s) where each Micron Accused Product was shipped from; (6) location(s) where each Micron Accused Product was shipped to; (7) location(s) where the title of Micron Accused Products was transferred or other locations where Micron and the purchaser agreed that a transfer takes place; (8) billing addresses; (9) locations where each Micron Accused Product was manufactured, assembled, and tested; (10) locations where the payment was made.

TOPIC NO. 44:

Micron's Documents relating to sales, costs, marketing, revenues, profits, expenses, and margins associated with sales of Micron Accused Products, including without limitation the content of such Documents, sources of data used to generate such Documents, how such Documents and information are created and maintained, and how the information within any such Documents is organized.

TOPIC NO. 45:

The facts and circumstances of all sales, or offers for sales of the Micron Accused Products, including but not limited to sales meetings in the United States, sales Communications to or from the United States, customization for the United States market, Communications with an entity whose parent is located in the United States, and any other sales activity occurring at least in part in or directed from or to the United States.

TOPIC NO. 46:

All facts and circumstances relating to the cost of researching, developing, testing, marketing, sourcing, sale, shipment, delivery, importation, or exportation by Micron in connection with each of the Micron Accused Product and the components thereof.

TOPIC NO. 47:

The date on and circumstances through which Micron began making, using, selling, offering for sale, or otherwise providing to a customer the first unit of each Micron Accused Product.

TOPIC NO. 48:

The expected, planned, and forecasted profitability, revenues, and sales of the Micron Accused Products.

TOPIC NO. 49:

Micron's past, present, and future assessment of its market share, state of competition, Competitors for Micron Accused Products.

TOPIC NO. 50:

All facts relating to any customer demand, request, discussion, interest, and requirements for Micron Accused Products in connection with the Patented Features, including any customer surveys, market research, or consumer research relating to Micron

Accused Products.

TOPIC NO. 51:

Micron's marketing, advertising, and promotion of the Micron Accused Products or the Patented Features, including without limitation all advertising or Communications between Micron and its past, current, and prospective customers about the value, advantages and importance of Micron Accused Products and the Patented Features comparing to others' competitive products.

TOPIC NO. 52:

Any research, analyses, studies, evaluations, opinions, competitive analysis, or any other activity Micron undertook or is undertaking to determine the past, current, or potential marketability, revenues, costs, profits, market share, or customer perceptions of Micron Accused Products including without limitation Micron's past, current, and future commercialization plans for Micron Accused Products.

TOPIC NO. 53:

The portion of the realizable profit from the sale of the Accused Products that should be credited to the alleged invention of the Netlist Patents-in-Suit as distinguished from nonpatented elements, the manufacturing process, business risks, or significant features or improvements added by Micron.

TOPIC NO. 54:

Micron's knowledge regarding all products that should be or should have been marked under the Netlist Patents-in-Suit.

TOPIC NO. 55:

Any products that practice or have ever practiced any claim of the Netlist Patents-in-Suit.

TOPIC NO. 56:

The Identity of any past or present DDR4 LRDIMM, DDR5 DIMM, or HBM product that does not practice any asserted claim of the Netlist Patents-in-Suit.

TOPIC NO. 57:

All facts relating to the appropriate amount of damages to which Netlist is entitled if the Netlist Patents-In-Suit are valid and infringed, including but not limited to any basis for Micron's contention that Netlist is not entitled to reasonable royalty in this case and/or basis for Micron's proposed royalty calculation, including facts applicable to each of the Georgia-Pacific factors and apportionment.

'TOPIC NO. 58:

The facts and circumstances relating to the preparation of any cost, revenue, profit, loss, or other financial Documents produced in this Action, including the meaning and interpretation of such financial Documents as well as the accuracy of the information contained therein.

TOPIC NO. 59:

For each Micron Accused Product sold worldwide since six years before the filing of this lawsuit, the total number of units manufactured, total number of units sold, gross and net revenue, costs (including total cost of manufacture, fixed costs, and variable costs), and gross and net profits, on a monthly and quarterly basis dating back to the date each Micron Accused Product was first sold, in each country, and Micron's systems and methods for tracking, recording, and maintaining such information. This should include data on transfer pricing between Micron entities. This should also include worldwide data because of any disputes regarding whether a product is sold or offered for sale or used in the United States. This should also include an explanation of how Micron attributes revenue from Micron Accused

Products to a particular country or region.

TOPIC NO. 60:

The facts and circumstances relating to how Micron determines or calculates rebates provided to customers, including but not limited to all reasons for which rebates are offered, how the amount of rebate is determined, who determines the amount of rebate, and how the amount of rebate may vary across customer, product, and time.

TOPIC NO. 61:

Micron's formal or informal policies, procedures, guidelines or practices for handling, negotiating, reviewing, editing, executing, or otherwise dealing with agreements relating to patent rights (including patent licenses), including what Person(s) at Micron is involved in or responsible for such agreements and the factors Micron considers when negotiating license agreements or attempting to determine the value of patents.

TOPIC NO. 62:

Micron agreements, contracts, patent licenses, or other licenses concerning any Micron Accused Product.

TOPIC NO. 63:

The shipment record of Micron Accused Products.

TOPIC NO. 64:

Any agreements, contracts, or licenses Micron contends are comparable to a license that Micron would have taken in a hypothetical negotiation in this case, including the facts and circumstances Micron took into account in considering or entering into any offer to license or purchase or any actual license or purchase agreement that Micron contends is reasonably comparable in scope to a license for the use or practice of any of the Netlist Asserted Patents.

TOPIC NO. 65:

All formal and informal indemnity agreements between Micron and any third party that relate in any way to Micron Accused Products, including the terms and circumstances of the agreements and all attempts to enforce the agreements.

TOPIC NO. 66:

Any competitive analysis or reverse engineering of any product manufactured, sold, or distributed by Netlist.

TOPIC NO. 67:

Any patent owned by Micron or third parties that covers the Accused Products.

TOPIC NO. 68:

The value contributed to Micron Accused Products separate from that recited in the claims of the Netlist Patent-in-Suit.

TOPIC NO. 69:

Micron's system(s) for tracking or recording patent licenses or other patent-related agreements to which Micron is or was a party, and any royalty payments made subject to those agreements, including but not limited to all lists, databases, or other compilations of such information.

TOPIC NO. 70:

All facts and circumstances relating to Micron's contention that any claim of the Netlist Patents-In-Suit is essential to practicing a standard, including the specific section of any standard being practiced.

TOPIC NO. 71:

Micron's awareness and/or knowledge of the Netlist Patents-In-Suit and of any patent application or patent relating to any of the Netlist Patents-in-Suit, including but not limited to

the date on which Micron first gained such awareness and/or knowledge and the facts and circumstances relating thereto.

TOPIC NO. 72:

The facts and circumstances relating to any actions undertaken by Micron in response to becoming aware of the Netlist Patents-in-Suit, being accused of infringement of Netlist's Patents-in-Suit, and/or of the Complaint in this Action.

TOPIC NO. 73:

Any evaluations, analyses, or other efforts by Micron to determine if any Micron Accused Product or any other Micron product would infringe the Netlist Patents-In-Suit, including the facts and circumstances of those efforts, the results of those efforts, any opinions of counsel relating to such efforts or patents, and any conclusion as to whether or not Micron needed or should obtain a license to one or more of the Netlist Patents-In-Suit.

TOPIC NO. 74:

All facts and circumstances relating to the basis for Micron's contention that Micron's infringement of the Netlist Patents-In-Suit has not been willful, including the facts and circumstances relating to the willfulness evaluation factors set forth in *Read Corp. v. Portec, Inc.*, 970 F.2d 816 (Fed. Cir. 1992).

TOPIC NO. 75:

Any effort made by, on behalf of, or at the request of Micron to design around and/or develop a non-infringing alternative to any or all of the Netlist Patents-In-Suit, including the facts and circumstances concerning such efforts, any reason for not implementing or deploying any design around or non-infringing alternative to the Netlist Patents-In-Suit, the existence or feasibility of implementing any such design around or non-infringing alternative, any plans or strategies for designing or developing any such design around or non-infringing

alternative, any benefits or disadvantages of any such design around or non-infringing alternative, and the costs, engineering requirements, and/or changes necessary to implement any such design around or non-infringing alternative.

TOPIC NO. 76:

The facts and circumstances relating to any policy in effect now or at any point, or any practice by Micron personnel, whereby Micron employees are discouraged or prohibited, or understand themselves to be discouraged or prohibited, from reading patents and/or patent applications filed by other companies.

TOPIC NO. 77:

Whether Micron instructs its employees on avoiding infringement of others' intellectual property, and the programs, policies, and steps employed towards such avoidance.

TOPIC NO. 78:

The facts and circumstances relating to any opinions of counsel upon which Micron intends to rely on in this Action.

TOPIC NO. 79:

The identification of any Micron employee who reviewed or analyzed any Netlist products, or Netlist presentations to Micron, involving or relating to a memory module involving DRAM, VLP RDIMMS, Rank Multiplied DIMMs, Planar-X RDIMMs, NVvault, EXPRESS VAULT, HyperCloud, HybridDIMM, or NVDIMMs, or memory packages with TSVs, the nature and date of the analysis, and all documents relating to the analysis.

TOPIC NO. 80:

The identification of any Micron patents that cover the Micron Accused Products.

TOPIC NO. 81:

Micron's policies practices, and procedures for document management, storage, and

preservation, including both paper and electronic documents.

TOPIC NO. 82:

For each Micron Accused Product, the JEDEC specification(s) such Micron Accused Products practice.

TOPIC NO. 83:

The role played by any Micron employees in JEDEC meetings regarding the design and function of the PMIC present on DDR5 modules, the adoption of distributed data buffers in DDR4 LRDIMMs, or the adoption of the Advanced Memory Buffer (“AMB”) for DDR2 FBDIMMs, and the identification of the Micron employees who first defined these features on Micron DDR5 products, Micron FBDIMMs, or Micron LRDIMMs.

TOPIC NO. 84:

Any industry standards or practices relating to the licensing of or royalties for memory module technologies.

TOPIC NO. 85:

Any factual bases for Micron’s statement that it has an express or implied license to any Netlist’s patents-in-suit.

TOPIC NO. 86:

Any factual bases for Micron’s laches, inequitable conduct, and unclean hands defenses in connection with the ’506 patent.

TOPIC NO. 87:

Any factual bases for Micron’s position that Netlist failed to offer Micron a license on reasonable terms and conditions free of unfair discrimination and that Micron is a willing licensee to Netlist’s Patents-in-Suit.

TOPIC NO. 88:

Any factual bases for Micron's affirmative defenses.

TOPIC NO. 89:

For each Micron Accused Product, all facts and circumstances relating to Micron's position that the Accused Product does not practice one or more claims of Netlist's Patents-in-Suit.

CERTIFICATE OF SERVICE

I hereby certify that, on May 15, 2023, a true and correct copy of the foregoing instrument was served or delivered electronically via email to all counsel of record.

/s/Yanan Zhao
Yanan Zhao